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Three level buck converter with improved dynamic performance using linear-non linear control

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Abstract: Dynamic response of a converter plays an important role in many applications which change load in a rapid manner, especially in PoL(Point of load)applications. Here a new method for improving the dynamic response of a converter is presented. Here separate control schemes are implemented during steady state as well as transient load conditions. A three level buck converter topology with fast transient response is discussed here. This topology does not require a soft start up circuitry for three level buck converter. Simulation model is done in Matlab/Simulink and the result shows a great improvement in dynamic response of the system.

Index Terms: Three level buck converter, dynamic response, transient response, soft start up.

I. INTRODUCTION

The dynamic response of a converter plays an important role in many areas like DSP based digital loads, point of load applications (PoL). Dynamic response is the performance of a converter during sudden load changes. The two important factors that should be considered during dynamic response are the peak overshoot as well as the recovery time. Many methods are proposed for improving the dynamic response of a system.

In [3], a converter with two control strategies is proposed. Pwm controller works at steady state condition and hysteresis controller which works at dynamic condition. Since hysteresis controller have its own disadvantages it is not suitable to use in all conditions. In [4] two buck converter topologies are cascaded each of them take care of two different conditions. The main disadvantage is that it requires more complex circuitry. A hysteresis controller is proposed in [6]. Some methods are proposed with change in the power stage of a converter to improve the dynamic response. In [7] a stepping inductance method is proposed. Here additional filter circuits are required and the system is complex as well.

Three level buck converter topology is proposed here. This topology reduces the switching stress, inductor size and has high efficiency [2],[8].

The buck converter circuit converts a higher dc input voltage to lower dc output voltage. A basic buck converter topology requires only one switch but it requires a large inductor value and switches work at very high frequency. So in the case of portable devices like mobiles the size should be less. In the case of multilevel converters [9], the switching frequency is reduced as well as the inductor size is also reduced, which in turn reduces the entire size of the converter as well.

In section II three level buck converter topology is discussed. Section III suggests its control schemes. Simulations results are discussed in section VI. Conclusion is presented in section V.

II. FLYING CAPACITOR THREE LEVEL BUCK CONVERTER TOPOLOGY

Three level buck converter works as a multilevel converter. The three level buck converters can offer high efficiency and high power density in voltage regulation and point of load applications. The gains are made possible by adding a flying capacitor that reduces the MOSFET voltage stress by half allowing for the use of low voltage devices, doubles the effective switching frequency, and decreases the inductor size by reducing the volt-second across the inductor. The flying capacitor three-level buck converter topology is illustrated in Fig.1.

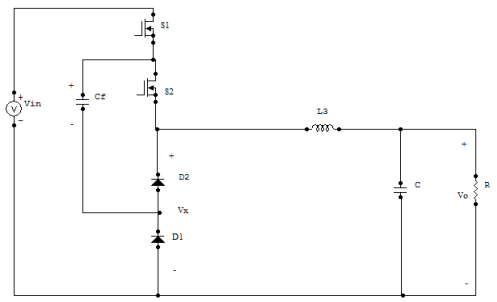

Fig.1- Flying capacitor three level buck converter

The switches s1 and s2 work complement to each other. In this topology, the converter can operate at three voltage levels (0, 0.5*V*in, *V*in). When switches *S*1and *S*2 are conducting, the capacitor is by passed and the entire input voltage will appear across the output and the inductor get charged and the inductor current raises to peak value. When switch *S*1and diode *D*2 are conducting the capacitor get charged and a difference of capacitor voltage as well as the input voltage will appear across the output. Similarly, when the switch S2 as well as diode D1 are conducting, the capacitor begins to discharge and the output voltage appear to be .5Vin. Finally, when diodes *D*1and *D*2 are conducting, the current free wheels and the inductor current discharges and the voltage across the output is 0. Because of the additional voltage level, the

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size of the inductor used in design of the converter is small for the same output current ripple.

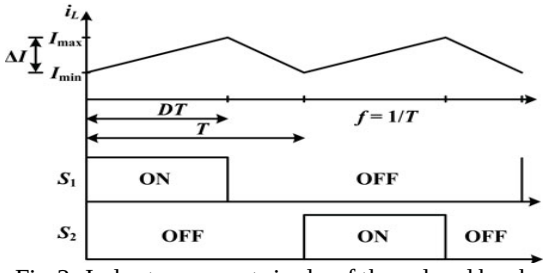

Fig.2 -Inductor current ripple of three level buck converter [1]

When duty ratio D<.5 the voltage levels obtaining are (0,Vin-Vc,Vc). The ripple current waveform is shown in fig.2. In this case the switching combination, S1and S2 turned on does not come into effect since the duty ratio is less hence no overlapping come into effect. From the waveform it is clear that the effective ripple frequency at the output is doubled. So that the switches are subjected to low voltage stress as well as the inductor size is reduced. The inductor ripple current is given by

$$\Delta i_L = \frac{V_{in}}{L.f}(.5 - D) \quad (1)$$

for D<.5, where D is the duty ratio and f is the frequency.
Thus the minimum inductance required for continuous conduction is

$$L_{\min} = \left(1 - \frac{2V_0}{V_{in}}\right)\frac{RT}{2} \quad (2)$$

Thus three level buck converter topology gives a reduced inductor size so that the overall size of the converter is reduced. Thus comparing with conventional buck converter the inductor size is reduced which gives a higher power density. The ripple current frequency is doubled, so that the switches are subjected to low switching frequency than that of conventional buck converter. The voltage stress across the switches is also reduced since the switches are only subjected to half of the input voltage.

In conventional buck converter when a load change occur it take some time to settle down to the new output. When there is a load step up change, switch S will be turned on. Thus the inductor slew rate is given by

$$\frac{di_L}{dt} = \frac{V_{in} - V_o}{L}, \quad (3)$$

where L is the inductance of buck converter.

When there is a load step down change occur, switch will be open and the inductor slew rate is given by

$$\frac{di_L}{dt} = \frac{-V_o}{L}, \quad (4)$$

where L is the inductance of buck converter.
In the case of three level buck converter, the inductor current slew rate for load step up and load step down is given by,

$$\frac{di_L}{dt} = .5V_{in} - V_o/L \quad (5)$$

And $\frac{di_L}{dt} = \frac{-V_o}{L}$ (6)

Here the inductor value is less compared to conventional converter hence the slew rate is increased in case three level buck converter in step down load change. The dynamic response of the system depends on the inductor current slew rate. The dynamic response of a system can be increased either by changing the power stage or by changing the control algorithm. The commonly used control methods for dc-dc converters are pulse width modulated (PWM) voltage mode control, PWM current mode control with proportional (P), proportional integral (PI), and proportional integral derivative (PID) controller. These conventional control methods like P, PI, and PID are unable to perform satisfactorily under large parameter or load variation. Therefore, nonlinear controllers come into picture for controlling dc-dc converters. The advantages of these nonlinear controllers are their ability to react suddenly to a transient condition. The different types of nonlinear controllers are hysteresis controller, sliding mode controller, boundary controller, etc. But they have many disadvantages also. In order to improve the dynamic response of converter in much more simpler manner a modified control scheme is proposed here. Here two control schemes are used in steady state and transient conditions. In transient condition a hysteresis controller used.

III. CONTROL STRATEGIES

A new transient controller is presented in this section. Fig. 6 depicts the diagram of the proposed control approach. There are three major blocks in the control scheme. First is the steady-state controller that could be any kind of voltage mode or current mode controller. The second major block is the transient detector. Load transients are detected by monitoring the current passing through the output capacitor (i_c).

Under steady-state conditions, the average value of this current is zero and its ripple is almost equal to the ripple of the inductor current. If the load's power demand suddenly decreases, the current of the capacitor starts rising. I_{cth+} is the threshold considered to detect a load step-down change. Also, if the load's power demand suddenly increases, the current of the capacitor starts falling. I_{cth-} is the threshold considered to detect a load step-up change. The selection of the threshold values depends on the capacitor current ripple, magnitude of load changes; and noise in the relating signals. Larger thresholds will result in additional detection delay and subsequently, affect the dynamic performance. On the other hand, if the threshold values are selected to be too close to zero, normal operation of the converter may falsely trigger the transient controller. One can easily find how much change should occur in the output load resistance so that it can be detected.

As shown in this figure7, under steady-state conditions, switches S1and S2are commanded by the steady-state controller. It is worth noting that this state of operation is also in charge of regulating the flying capacitor voltage.

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When a load step down occurs and capacitor current i_c gets greater than threshold i_{cth+}, the transient will be detected. Then the control scheme is shifted to hysteresis controller. For the simple design of the proposed controller, the transient control is switched back to the steady-state control by the zero detection of the capacitor current. Similarly, if there is a load step up and capacitor current i_c get less than threshold i_{cth-}, the transient will be detected. Again the control scheme is changed to hysteresis controller. The transient control is switched back to steady-state control by the zero detection of the capacitor current.

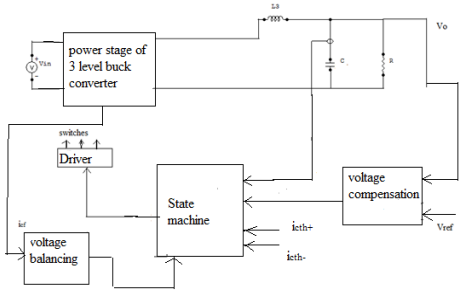

Fig 6- Control strategy

Fig.6 shows the control block diagram. It mainly consists of three sections, transient detection, state machine as well as flying capacitor voltage balance.

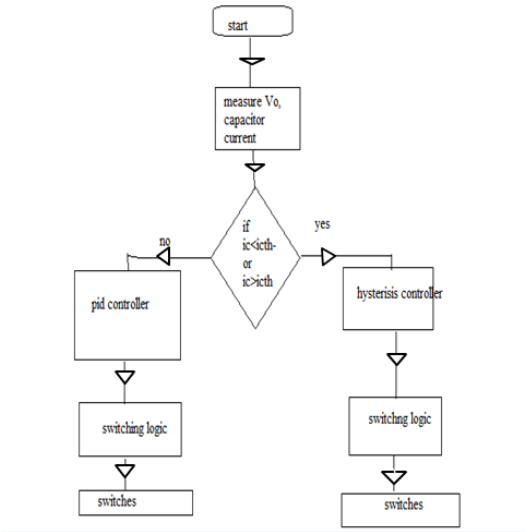

Fig 7-Logic implementation

The steady-state controller could be any kind of voltage mode or current-mode controller and the output of the steady-state controller are the three control signals for switches *S*1, *S*2 . Here a PID based voltage controller is used. In order to detect the load transient change, the capacitor current is compared with threshold values of capacitor current. If a step up load change is detected, that is if the capacitor current goes beyond the threshold value then the three switches are kept on for the entire period in which the current settle down. Similarly switches are kept off in the case of a step down load change.

The three level converter work properly only if the flying capacitor voltage remains at half of the input voltage for the entire working time. Theoretically, it is achieved by keeping the two switches work complement to each other. But in practical condition it is not achieved due to parasitic and thus a controller is necessary for the operation. The voltage balancing can be implemented as in fig.9.

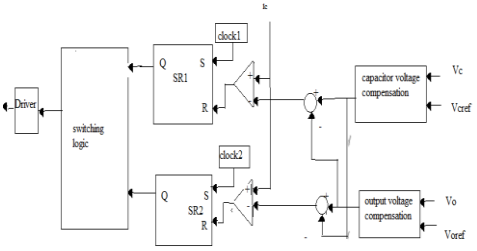

Fig 8 -Voltage balancing circuit

Here capacitor current is used to achieve voltage balancing. Here the capacitor voltage is compared with the reference voltage and the error thus obtained is fed to a pi controller and along with that the output voltage error is also taken into account. The control signal achieved from the controller is then compared with current drawn and the output thus obtained is used to drive a SR flip flop. Thus the switches are controlled to achieve voltage across the capacitor to be half of the input voltage. The proposed scheme does not require phase shifted ramp signals. It requires only the knowledge of capacitor current.

IV. SIMULATION RESULTS

The buck converter is simulated in closed loop configuration. The duty ratio is 25% and hence for an input of 24V an output voltage of 6V is obtained. The switches work at a phase shift of 180 degree. A variable delay is provided, so that the two switches work with a delay of 180 degree. Three level buck converter works as a simple buck converter with three voltage levels Vin-Vc,Vc,0 when the duty ratio is less than .5 and it works with voltage ranges Vin,Vin-Vc,0 when duty ratio is greater than .5 The closed loop is obtained by providing a PID controller in the feedback path. Outer control loop as well as inner control loop is used. The output voltage is made constant by comparing it with reference voltage and it is passed through a PID controller to obtain the reference current. Manual tuning is done for getting the values of Kp and Ki of PI controller.

The parameters used are input 24V, output 6V, switching frequency 100kHz. The entire simulation diagram is shown in fig 9.

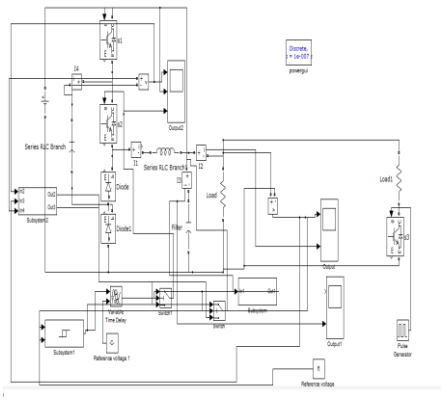

Fig 9 simulation diagram

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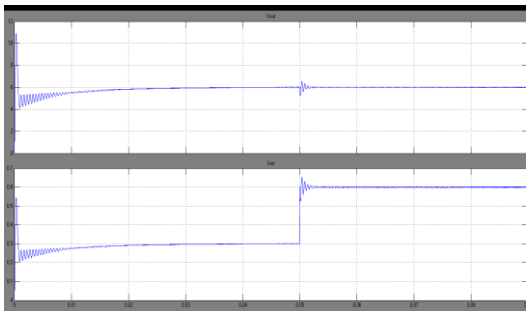

Fig.10- Output of closed loop buck converter

Fig.10 shows the output of the three level closed loop buck converter. From the output diagram it can be seen that after a transient, it takes almost 5 cycles to come to the steady state position. During the initial condition the starting voltage goes up to 11V which should be reduced otherwise the switches will be subjected to high voltage. At time .005seconds a load change is occurred. Hence the current raises and takes some time to settle. The settling time is found to be 250µs.

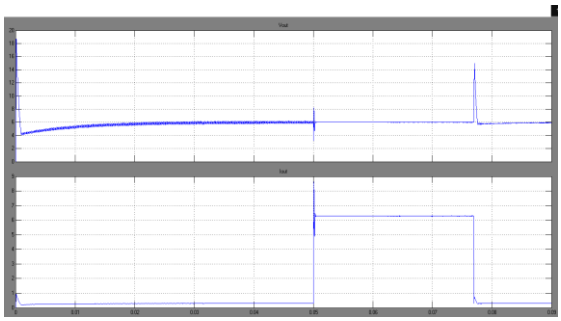

Fig 11-Output waveform for modified controller

Fig 11 shows the simulation of three level converter with hysteresis controller in transient condition, ie the output of modified controller without voltage balancing circuit**.** Here the settling time in step up condition is reduced to 50µs.. Fig 12 shows the output after applying the voltage balancing circuit.

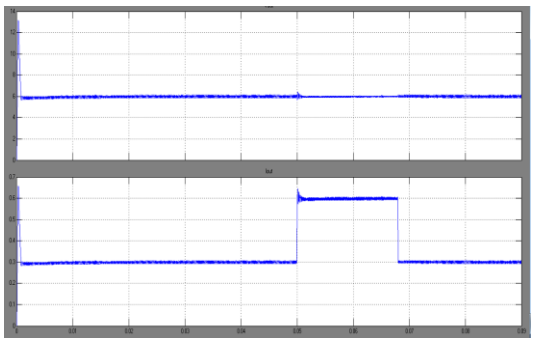

Fig 12-Output waveform for converter with voltage balance

The settling time has been reduced to less than 20µs. From fig. 12 it can be seen that the settling time for converter has been reduced considerably with voltage balance. It can be also shown that the peak overshoot of voltage has been considerably reduced with converter when provided with voltage balance. Here at the initial stage the converter is subjected to low voltage compared to conventional converter topology. Hence separate soft starting circuit is not necessary for three level buck converter topology.

V. CONCLUSIONS

A transient control strategy to improve the dynamic response of a flying capacitor three-level buck converter has been proposed. Two control schemes are used in transient and steady state condition. In transient condition hysteresis controller is used and a PID controller is used in steady state controller. A voltage balancing circuit has been proposed for the flying capacitor output voltage. Simulation results show that the proposed approach can greatly improve the dynamic response for both load step-up and load step-down scenarios. Comparing with other methods, the proposed controller has advantage of both faster dynamic response performance and simpler control structure. Filtering capacitor required is less due to small variation in output voltage. Here the three level buck converter is subjected to low voltage in the starting time as well so it does not require any additional soft start up circuitry.

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